WHAT IS CLAIMED IS:

1. A programmable logic device (PLD) comprising:

input/output (I/O) interface having a first plurality of I/O register blocks, the first plurality of I/O register blocks being partitioned into a second plurality of I/O sections each I/O section having N data I/O register blocks and a strobe circuit, wherein each of the N data I/O register blocks is configured to store multiple bits of data, and each strobe circuit is configured to generate a local strobe signal that drives a local clock line coupling to clock inputs of the N data I/O register blocks, the N data I/O register blocks and the strobe circuit in each I/O section being coupled to a corresponding number of device pins; and

programmable logic circuitry coupled to the I/O interface.

2. The PLD of claim 1 wherein the strobe circuit in each I/O section is configured to shift a phase of an input strobe signal received at a respective strobe pin.

3. The PLD of claim 2 further comprising a master phase control circuit coupled to receive a master clock signal and configured to generate a phase control signal that controls a phase delay in the strobe circuit in one or more of the second plurality of I/O sections.

4. The PLD of claim 3 wherein the second plurality of I/O sections are grouped into a third plurality of I/O banks.

5. The PLD of claim 4 wherein a separate master phase control circuit is provided for I/O sections in each of the third plurality of I/O banks.

6. The PLD of claim 1 wherein each I/O register block comprises two registers, one of which stores a first incoming bit of data at a rising edge of the local strobe signal and the other stores a second incoming bit of data at a falling edge of the local strobe signal.

7. The PLD of claim 6 wherein the strobe circuit in each I/O section comprises a programmable phase delay circuit that is configured to shift a phase of the local strobe signal such that an edge of the local strobe signal occurs substantially at the center of a data pulse.

8. The PLD of claim 7 wherein the phase delay is about 90 degrees.

9. The PLD of claim 1 wherein each I/O section further comprises one or more general purpose register blocks coupled to respective device pins.

10. The PLD of claim 1 wherein, in each I/O section, the strobe circuit is located as close to a center the N data I/O register blocks as possible wherein an equal number of data I/O register blocks are located in either sides of the strobe circuit.

11. The PLD of claim 1 wherein the programmable logic circuitry comprises a plurality of programmable logic blocks coupled via a network of a plurality of programmable vertical and horizontal interconnect lines.

12. A computing system comprising a multiple-data-rate memory circuit coupled to a programmable logic device (PLD) as set forth in claim 1.

13. The computing system of claim 12 wherein the multiple-data-rate memory circuit comprises a double data rate synchronous dynamic random access memory.

14. A method of operating a programmable logic device (PLD) comprising:

receiving N groups of data bits each group having M data signals and a corresponding data strobe signal;

partitioning I/O register blocks inside the PLD into a corresponding N I/O modules, each module having M I/O register blocks and a strobe circuit coupled to receive a respective group of M data signals and data strobe signal; and

driving clock inputs of the M I/O register blocks in each of the N I/O modules using an independent clock network that is local to each of the N I/O modules.

15. The method of claim 14 further comprising programmably shifting a phase of the data strobe signal before driving the clock inputs of the M I/O register blocks.

16. The method of claim 15 wherein the programmably shifting of the phase of the data strobe comprises generating phase control signal in response to a system clock.